ABSTRACT OF THE DISCLOSURE

[0095] A synchronous DRAM is provided which includes arrangements for operations of power supply circuitry based upon whether the DRAM is in a power down mode or not. In one embodiment, a first power supply circuit and a second power supply circuit are provided which both receive externally supplied voltages and output internal supply voltages. The first power supply circuit is not in operation when a semiconductor device of the synchronous DRAM is in a power down mode. However, the second power supply circuit is continuously in operation during the power down mode. In another arrangement, the operation of a voltage limiter circuit is controlled based on whether or not the DRAM is in a power down mode.